EPFL

MICRO-331
Microfabrication technologies

Lecture 2

Yujia Zhang

2025 edition

Today's program

- 1st hour:
  - Feedback of the SLT_1 (8')
  - Feedback and update on the AI tutor (2')
  - Recapitulation: MEMS (10')
  - Recapitulation: Cleanroom (10')
  - Process flow (10')
  - Q&A (5')
- 2nd hour:
  - Chemical vapor deposition (CVD) (40')
  - Q&A (5')

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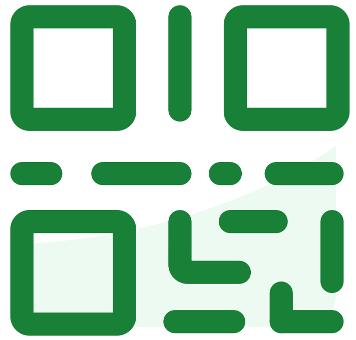

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Yujia Zhang

1 Microfabrication technologies
5 YZ

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Feedback of the SLT_1

- What was your experience when **preparing** for the first SLT?

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What was your experience when preparing for the first SLT?

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Speaker

Feedback of the SLT_1

- What was your experience **during** the first SLT?

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What was your experience during the first SLT?

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Speaker

Feedback of the SLT_1

- What was your impression **after** the first SLT?

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What was your impression after the first SLT?

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Speaker

Feedback of the SLT_1

- Any suggestions, comments, things to be improved?

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Audience Q&A
Any suggestions, comments, and things to be improved?

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Feedback and update on the AI tutor

- Any questions when using the AI tutor?
- Fasten seat belt: AI Tutor BOT now in ‘adventurous' mode

Recapitulation: MEMS & Cleanroom

Speaker

Recapitulation: MEMS & Cleanroom

- What are MEMS?
  - **M**icro-**E**lectro-**M**echanical **S**ystems
    - Microsystems
    - **Microfabrication**
    - **Microtechnology**
    - Nanotechnology
    - …

MICRO-331

- **Microfabrication is a manufacturing technology**
  - A way to make micro-stuff
  - Adapted from the semiconductor industry (Integrated Circuit, IC)
    - Therefore, many standard design **principles** hold
    - **With changes!**

A comparison between IC and MEMS fabrication steps

- IC
  - Silicon doping
  - Silicon oxidation
  - Thin film deposition
  - (CVD/PVD)
  - Photolithography
  - Thin film etching
  - (dry/wet)
  - …

Nothing moves !!

- MEMS
- Create mechanically freestanding and movable elements for physical **sensing** or **actuation**. For example:
  - Accelerometers
  - Microphones
  - Bulk Acoustic Wave resonators
  - Bi-morph micro-actuator

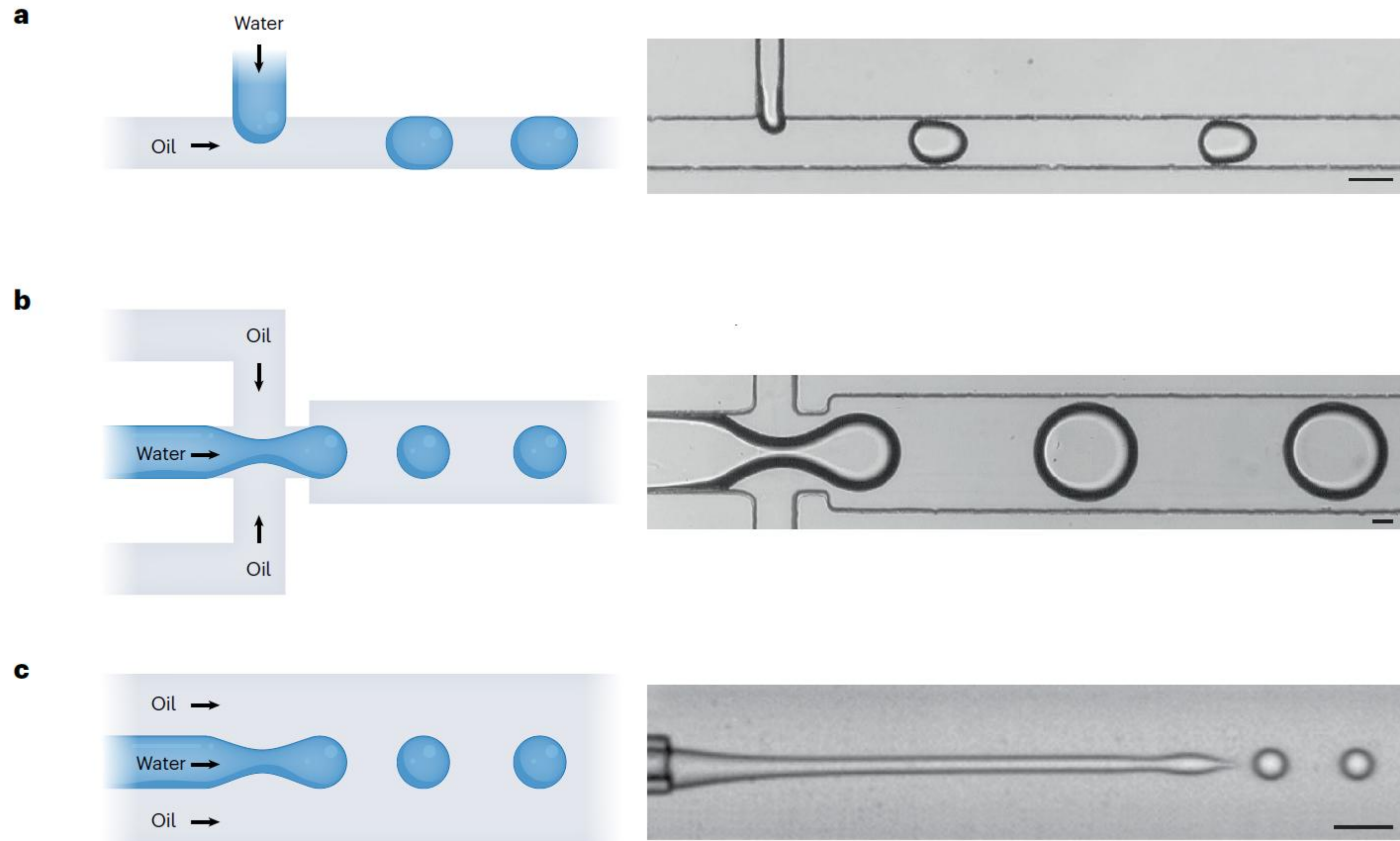
See MOOC:
Successful MEMS + Bimorph case study

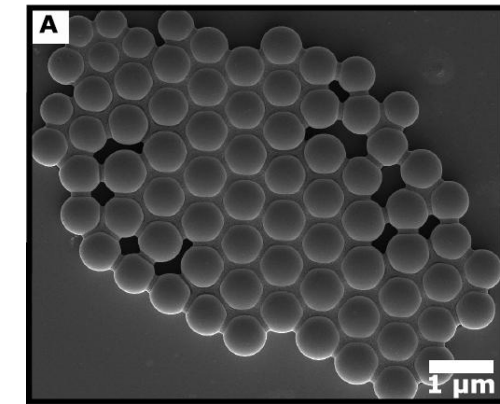
AI: The key difference is that Integrated Circuits (ICs) are purely electronic, processing and controlling signals, while Micro-Electro-Mechanical Systems (MEMS) combine electronic and mechanical components to sense or actuate physical quantities like pressure or motion. ***ICs are like the "brain," handling data, whereas MEMS act as the "eyes" and "arms," interacting with the physical world.***

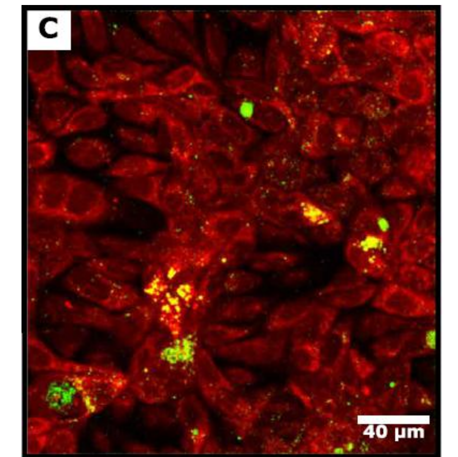
- Reference to Lecture 1, Slide 19

However, definitions can evolve

- **Now, many 'M~~EM~~S' have no 'E' or 'M'**
- **For example:**
  - Microfluidic systems







Nat Rev Methods Primers **3**, 32 (2023); *Sci. Adv.* 2020; **6** : eaay7952;

Emerging technologies & new opportunities for MEMS

8.01 **Quantum Devices and Systems** with MEMS/NEMS
8.02 Internet of Things (IoT) with MEMS/NEMS
8.03 Nonlinear Dynamics in MEMS/NEMS
8.04 New Computing Devices and Systems with MEMS/NEMS
8.05 **Machine Learning (ML) & Artificial Intelligence (AI)-Enhanced** MEMS/NEMS Design, Manufacturing, and Applications
8.06 MEMS/NEMS for the **Hardware of AI, Virtual Reality, Augmented Reality**
8.07 MEMS/NEMS for Hardware Security (e.g., Electronic Circuits, Systems)
8.08 MEMS/NEMS for Advancing Scientific Instrumentation and Metrology

https://mems26.org/

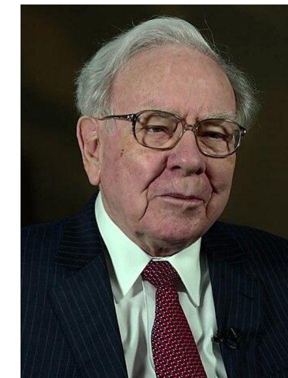
A balance between academic curiosity and commercial success

- Science:
  - Approaches to prepare tiny materials for testing (e.g., nanofluidic channels)
  - Interesting effects at the micro-/nano-scale
  - Unique application scenarios, i.e., minimally invasive implants, ultra-low-power sensors, etc

  …

- Commercialisation:
  - Huge markets: automobile industry, medical implants…
  - **Smaller** components mean a **higher integration** level, e.g., a smartphone
  - **Scale-up production** means **cheaper** than alternatives, e.g., glucose monitors

  - Tbh, it's challenging to design and more challenging to fabricate (batch-to-batch variation)
    - low successful rate → high cost
  - Unforeseen issues related to system **connection** (to other components) and **packaging**
  - Cleanroom → very high cost
  - But if it works, then you have an **Economic Moat**



Cleanroom

- Why do we need a cleanroom?

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Why do we need a cleanroom?

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Speaker

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What is the ISO class of the CMi at EPFL?

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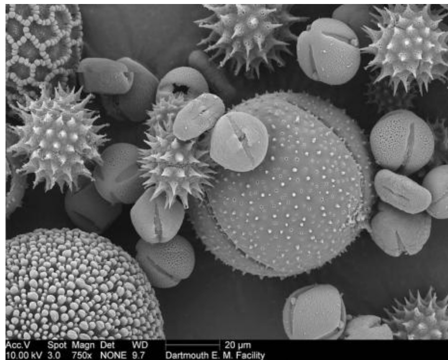
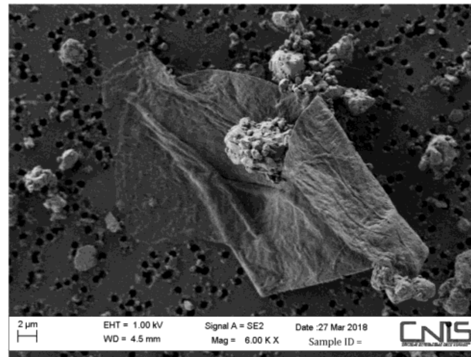
ISO 14644

- ISO 14644 is the international standard used to design, construct, validate and operate a **cleanroom**.
- ISO 14644-1:2015 specifies the classification of air cleanliness in terms of concentration of **airborne particles** in cleanrooms and clean controlled environments.



Pollen



Skin dust

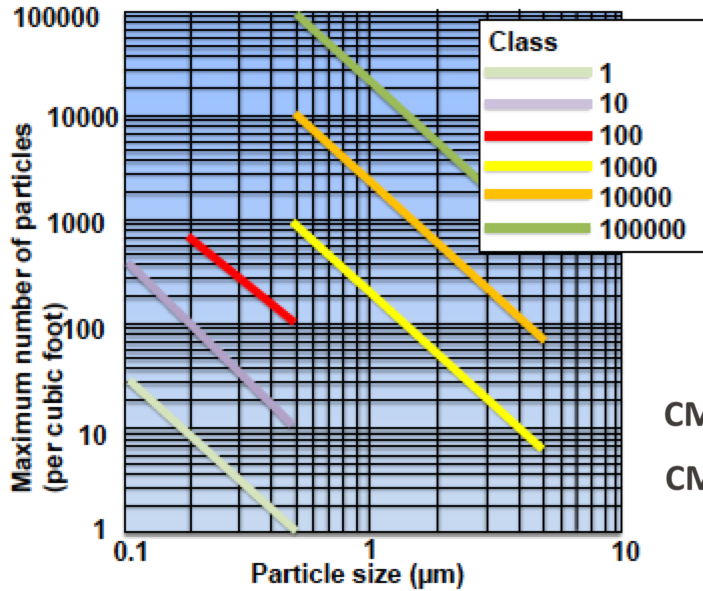
Cement dust

Unwanted ions and chemicals, etc

https://en.wikipedia.org/wiki/Particulate_matter

ISO Classification

- ISO class 1: 10 particles per m³ (particles > 0.1µm)
- ISO class 5: 100,000 particles per m³ (particles > 0.1µm)



CMi BM -1 ⟹ ISO 5

CMi BM +1 { ISO 6, ISO 7

Concentration max allowed of particles (particles/m³ of air)
Particles sizes equal or superior to that given below

Class ISO	0.1 µm	0.2 µm	0.3 µm	0.5 µm	1 µm	5 µm	Class US FS209 (0.5um particles/ft³ of air)
ISO 1	10	2	0	0	0	0	
ISO 2	100	24	10	4	0	0	
ISO 3	1 000	237	102	35	8	0	1
ISO 4	10 000	2 370	1 020	352	83	0	10
ISO 5	100 000	23 700	10 200	3 520	832	29	100
ISO 6	1 000 000	237 000	102 000	35 200	8 320	293	1 000
ISO 7	∞	∞	∞	352 000	83 200	2 930	10 000
ISO 8	∞	∞	∞	3 520 000	832 000	29 300	100 000
ISO 9	∞	∞	∞	35 200 000	8 320 000	293 000	

Standard ISO 14644-1

Information from CMi

EPFL

Contamination problems in microfabrication

- Device processing yield
- Device performance
- Device reliability

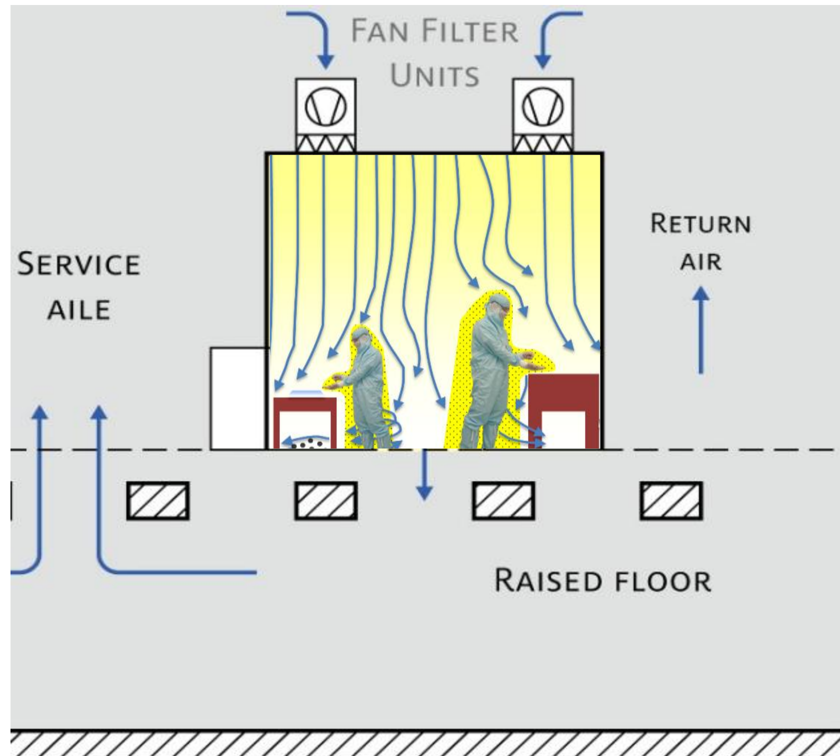
…

See MOOC:
Cleanroom basics and CMi overview

Cleanroom is a highly controlled environment

Air filtration

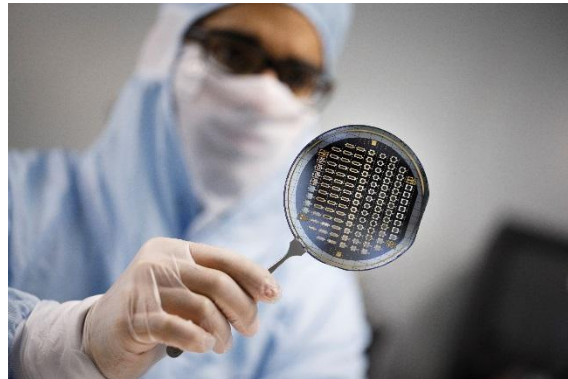
- Continuous air supply through filters. Laminar flow top to bottom.
  - HEPA (High Efficiency Particulate Air) or ULPA (Ultra-low Penetration Air) filters
  - Constant air flow: 20 to 600 air changes per hour
  - **Positive** air pressure



Information from CMi

Cleanroom is a highly controlled environment

- **Temperature** and **humidity** control
  - 20 – 24°C (stability of photolithography)
  - 40 – 60% RH
- Tight control of **media**:
  - Water (minerals, particles, dissolved ions)
  - Chemicals (purity, mobile ions)
  - Gas (purity, water vapour content, particulates)
- Special **cloth**, compatible **tools**, and lint-free paper, etc
  - Surface cleanliness
  - Equipment and tools designed to minimise particle shedding
  - Stainless steel, coated plastics, lint-free cloths

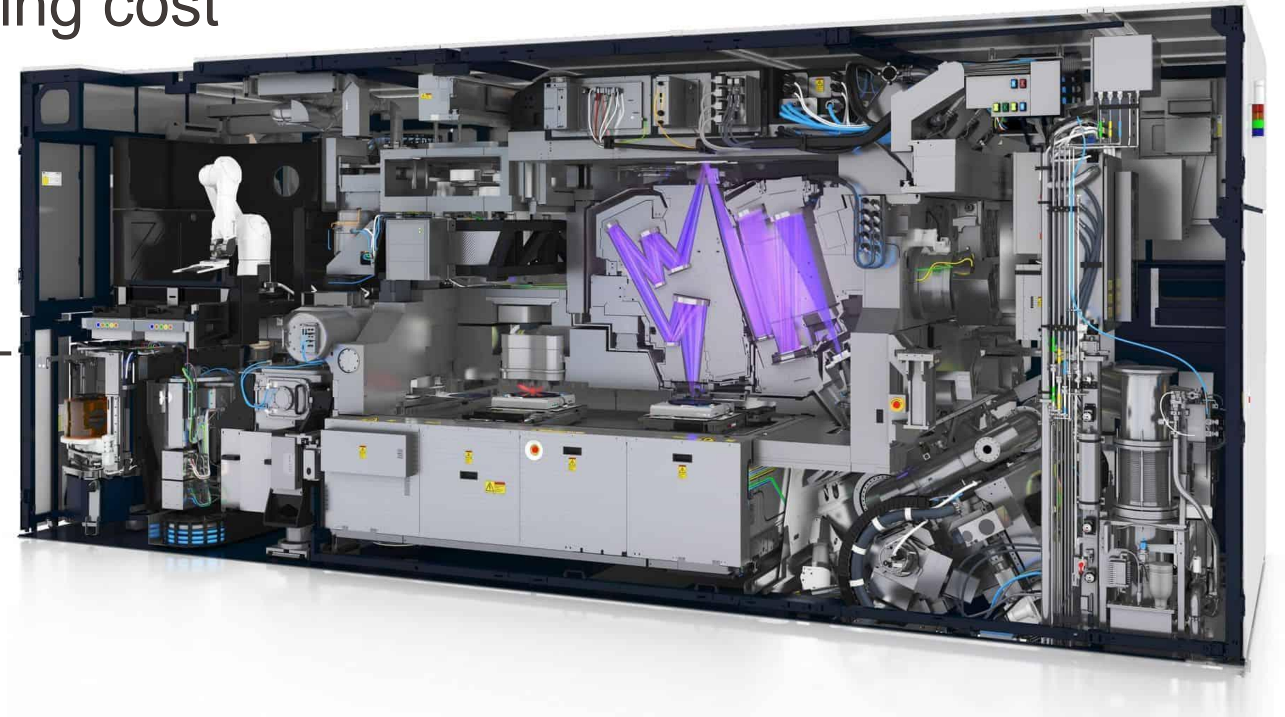


- Information from CMi

Other aspects of a cleanroom

- Huge capital investment and running cost

EUV Machines
~$400 Million
Image from ASML



- High **Carbon Footprint**

EPFL's Carbon Footprint

Night View © EPFL Jamani Caillet

Please visit
https://www.epfl.ch/about/sustainability/strategy/carbon-footprint/
to know more

YouTube: How ASML Makes Chips Faster With Its New $400 Million High NA Machine

Process flow

Speaker

What is a process flow?

- A process flow is like following a recipe: you combine the right ingredients in the right order and under the right conditions, building step by step—just like making a pizza.
- If you can design process flows in micro-/nanofab, you'll be in high demand in both research and industry, or even in *Michelin-starred restaurants* (*e.g.*, *molecular gastronomy*).

See MOOC:
Bimorph case study
for an exemplary process flow

- Reference to Lecture 1, Slide 22

Learning to ‘speak’ microfabrication

- ***Vocabulary***: common techniques, e.g., thin-film depositions by CVD/PVD, lithography, etching, etc.
  - *There are huge lists of things that you can and can’t do in microfab*
- ***Grammar***: detailed sequence of steps and techniques
  - *There are limits on how you can combine steps together to form a process*
- ***Fluency:*** only practice will make you fluent!
  - *An experienced microfabricator knows most of these capabilities and limits from long experience*
- **Our goal**: teach enough vocabulary and grammar to get you started.
  - Today starts with vocabulary CVD

Reference: Design and Fabrication of MEMS Devices, Spring 2007. MIT

Example of a process flow from the CMi

- A process flow example from BION

Today's program

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- 2nd hour:
  - Chemical vapor deposition (CVD) (40')
  - Q&A (5')

Chemical Vapour Deposition (CVD)

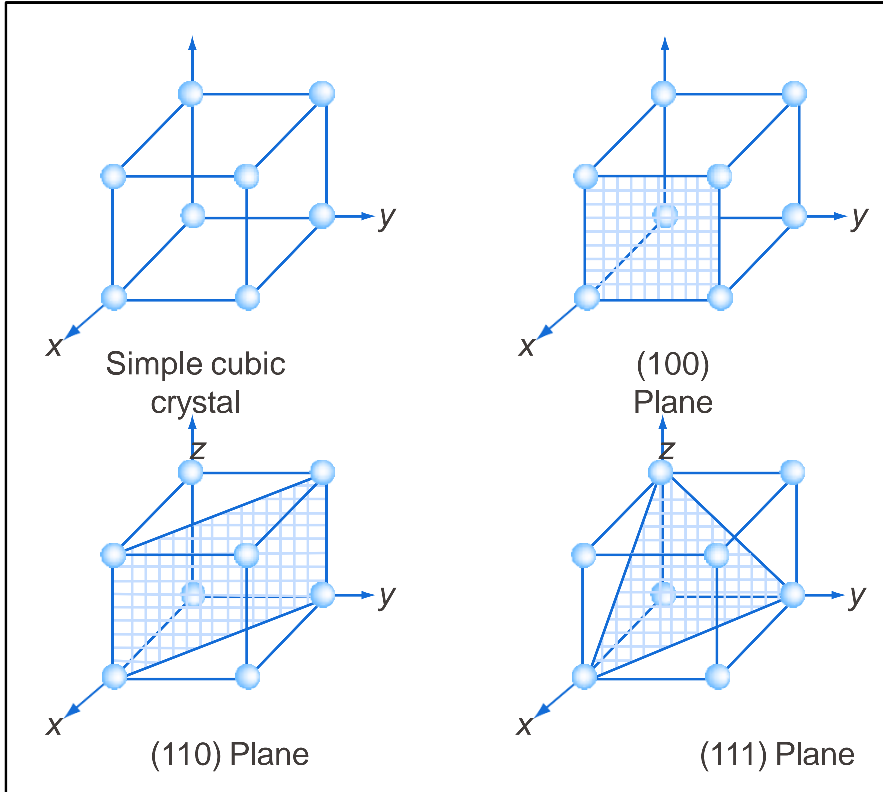
Speaker

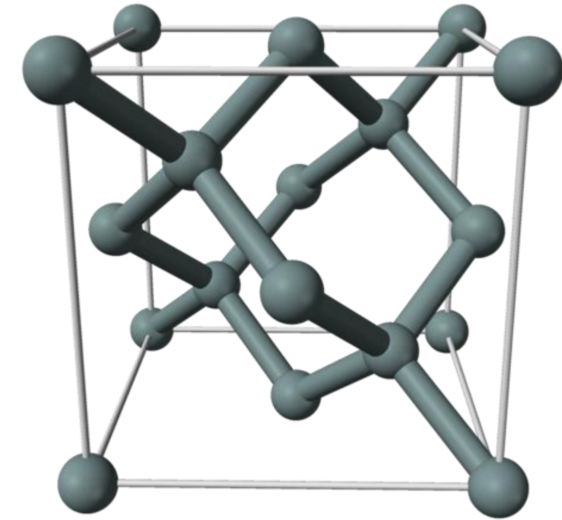
Key information of CVD

- **Chemical reaction** is involved
- Use of **gaseous** phase results in conformal **deposition** on substrate with arbitrary texture
- The goal is to create thin (or thick) films on the substrate (e.g., Si)
- Many techniques to choose from, so we should consider:
  - Quality of resulting films (electrical properties, etch selectivity, defects, residual stress, etc)
  - Conformality
  - Deposition rate
  - Cost
- CVD
  - Reactants are transported to the substrate, a chemical reaction occurs, and the products deposit on the substrate to form the desired film
- Physical techniques (Lecture 3)
  - Material is removed from a source, carried to the substrate, and dropped there

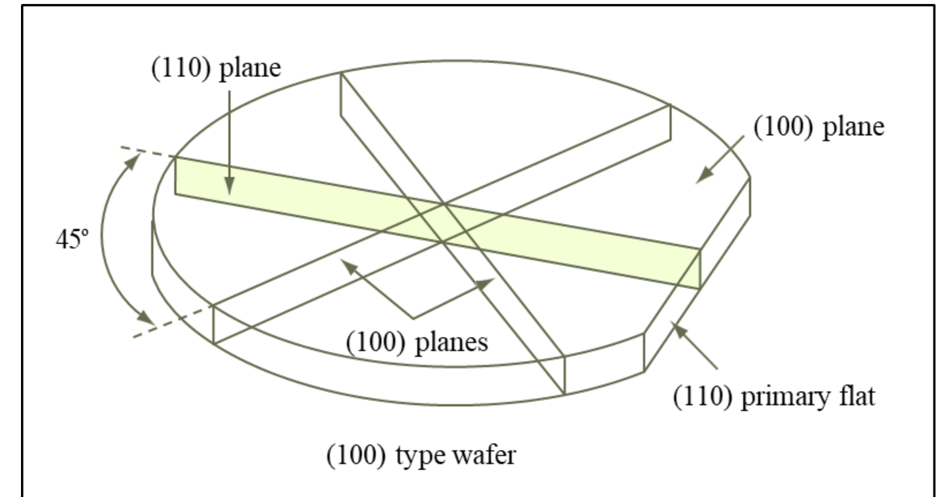
Preliminary knowledge before diving into CVD

- Silicon Wafers
  - Silicon is a diamond-structure cubic crystal





Diamond cubic crystal structure of a silicon unit cell



Wafer orientation

We will revisit this in Etching

Reference: Design and Fabrication of MEMS Devices, Spring 2007. MIT

Other substrates

- Si wafers with embedded layers, such as silicon-on-insulator (SOI) wafers
  - Initial purpose: build IC's on device layer, and buried oxide minimizes stray capacitance to substrate

- Silicon Carbide (SiC) wafers, wide bandgap semiconductor, use in electronic applications under extreme conditions
- Quartz (ordered atomic structure) / Glass (cheap, high impurity content)
  - Inexpensive base for soft lithography
  - Transparent for optical access
  - Can be very strongly attached to silicon wafers via anodic bonding
- Compound semiconductors (III-V's, II-VI's)
  - Optical applications
- Sapphire
  - Strong, wear resistant, transparent, insulating substrate
  - Expensive, hard to etch

Wafer doping

- Doping is the introduction of a controlled amount of impurities to change the conductivity type and degree of a semiconductor
- In silicon, boron is a p-type dopant (creating holes), while phosphorus, arsenic, and antimony are n-type dopants (creating conduction electrons)
- Some doping incorporated in the initial silicon melt
- All modern thin-film doping is done with ion implantation
  - A high-voltage accelerator is used to shoot ions at the wafer
  - The depth of the implant dose depends on energy
  - Activation anneal after implantation allows dopants to reach proper positions in the crystal (diffusion)
- Doping doesn't add a new thin film, but it modifies the properties of a thin film at the surface of existing material

You may learn more details in courses related to Semiconductor Physics and Devices

Reference: Design and Fabrication of MEMS Devices, Spring 2007. MIT

Now we are back to CVD

Taxonomy of deposition techniques

See MOOC:
Overview of CVD techniques

- *Thermal Oxidation*
- Classification of CVD by pressure
  - Atmospheric pressure CVD (APCVD)
  - Sub-atmospheric pressure CVD (SACVD)
  - Low-pressure CVD (LPCVD)
  - Ultrahigh vacuum CVD (UHV/CVD)
- Classification of CVD by reactor type (*not very often*)
- Other CVD
  - Plasma-enhanced CVD (PECVD)
  - Metal-organic CVD (MOCVD)
  - Atomic layer CVD (ALCVD or ALD)
- Epitaxy
- Electrodeposition (Electroplating)

Not mentioned in MOOC but very useful!

Thermal Oxidation

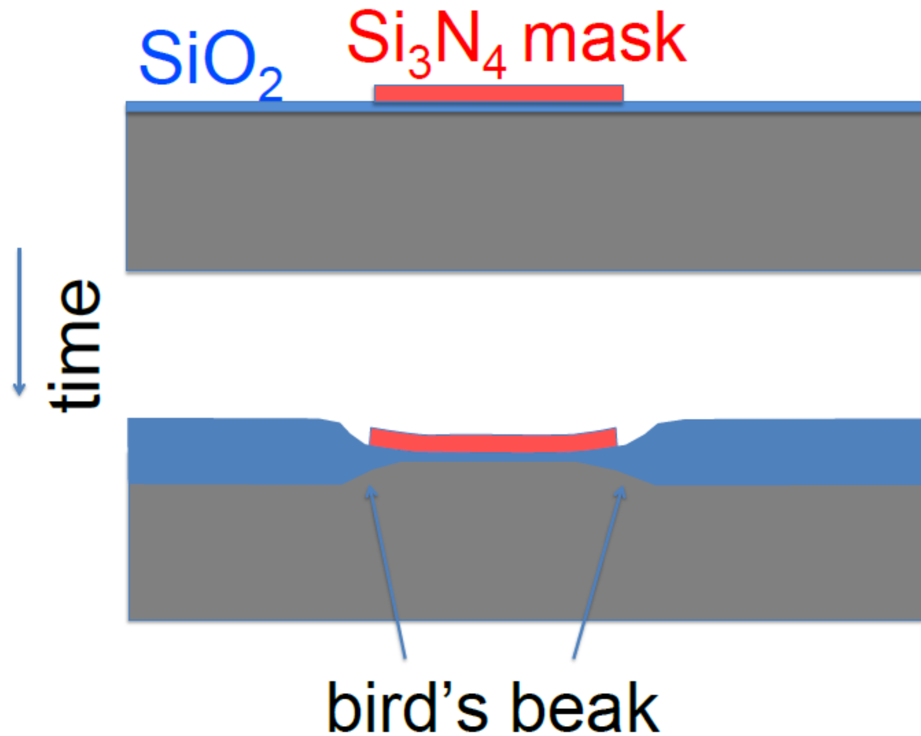
- Silicon transforms into silicon dioxide (SiO_2), also known as silica
- How it works:
  - Oxygen diffuses through oxide to Si/oxide interface (rate determination)
  - Diffusion limits practical oxide thickness to < 2 µm
  - Si + O_2 at high temperature → SiO_2
  - **Some Si is consumed, which makes it not truly a deposition!**
- Dry oxidation (O_2) $Si\ (s) + O_2\ (g) \Rightarrow SiO_2\ (s)$
  - Slow oxidation rate, smaller maximum thickness, higher quality
- Wet oxidation (H_2O steam) $Si\ (s) + 2\ H_2O\ (g) \Rightarrow SiO_2\ (s) + 2\ H_2\ (g)$
  - Faster oxidation rate, lower quality

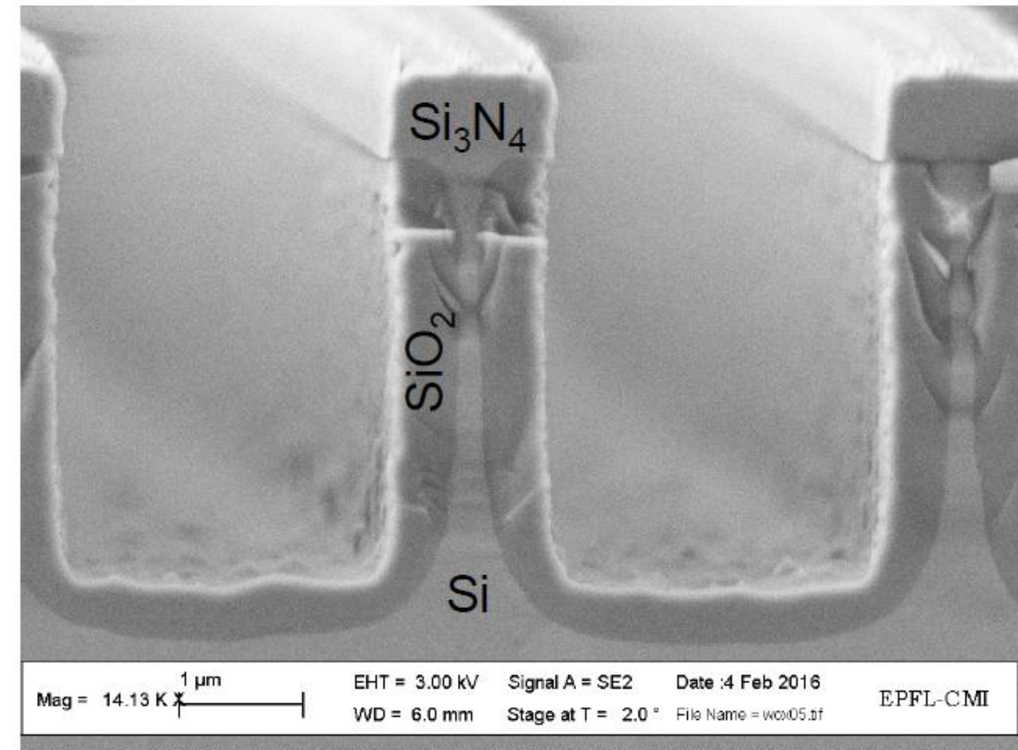
See MOOC:
Overview of CVD techniques
Specific CVD processes

The *Deal–Grove model* describes the growth of an oxide layer on the surface of a material.

Local oxidation of silicon (LOCOS)

- Oxidation can be masked locally by an oxidation barrier, such as Si_3N_4
- Oxide undercuts the edge of a mask layer to form a 'bird's beak'
- Oxidation followed by oxide etch can also be used to sharpen silicon features.





Some reasons to use CVD

- Oxide formation:
  - To get a thicker layer than thermal oxidation can provide
  - To create oxide on a wafer that can't withstand high temperatures
    - For example, because of metal features
  - To create oxide on top of a material that is not silicon
- For film formation in general:
  - To tailor the film properties (like film stress) by adjusting pressures, flow rates, external energy supply, ratios of different precursor gases (to adjust proportions of different materials in the final product)
  - Conformality: (more or less) even coating on all surfaces
  - To create thick films on the wafer surface

See MOOC:
Theoretical aspects of CVD

- Drawbacks
  - Films deposited at low temperature are often lower quality than high temperature versions, and have less predictable properties
  - Flammable, toxic, or corrosive source gases

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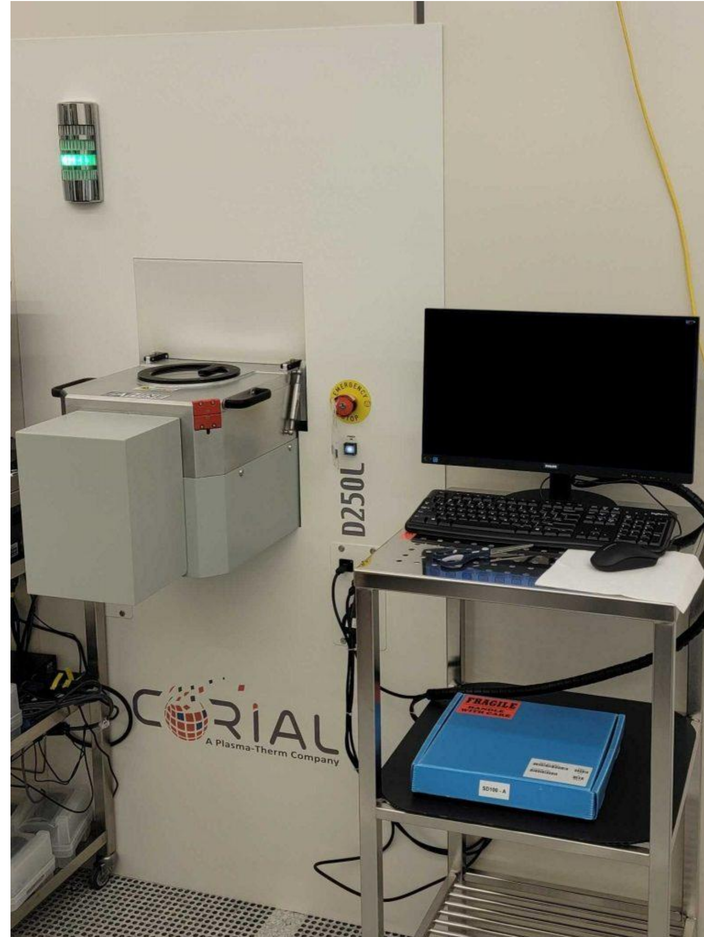
CVD is about chemical reactions

- **Unlike oxidation, it does not consume substrate material**
- Gaseous reactants, often at low pressure
  - Long mean free path*; reactants reach substrate
- Reactants react and deposit products on the substrate
- Commonly deposited films: Oxide, silicon nitride, polysilicon
- How to facilitate chemical reactions:
  - High temperature, plasma, laser
  - Processing temperatures vary widely
- **CVD results depend on pressures, gas flows, and temperature**
- Film composition, uniformity, deposition rate, and electrical and mechanical characteristics can vary

*The mean free path is the distance a particle will travel, on average, before experiencing a collision event.

CVD equipment in the CMi

Centrotherm furnaces, 15 tubes in 4 stacks

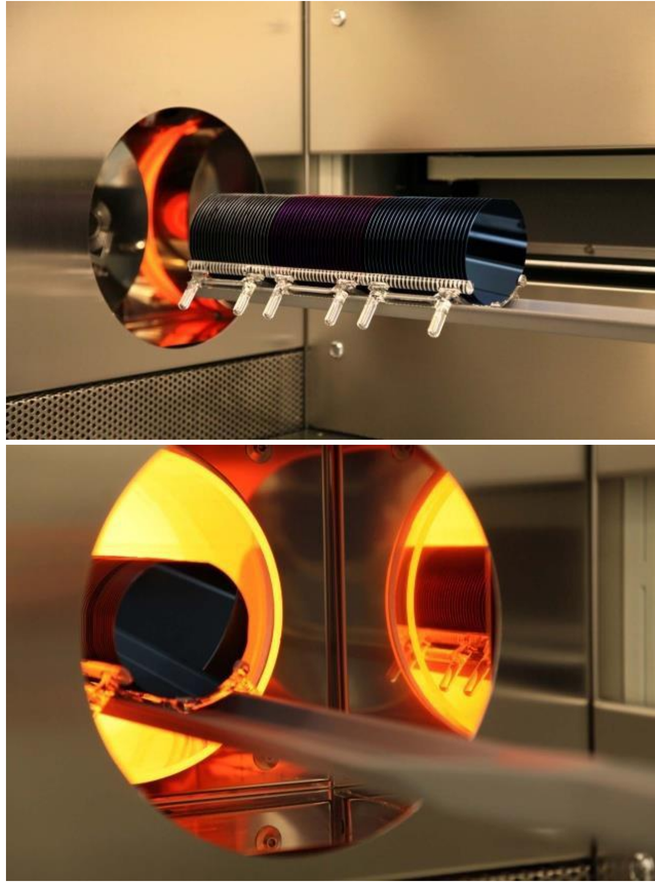


Plasma-Therm Corial D250L – PECVD

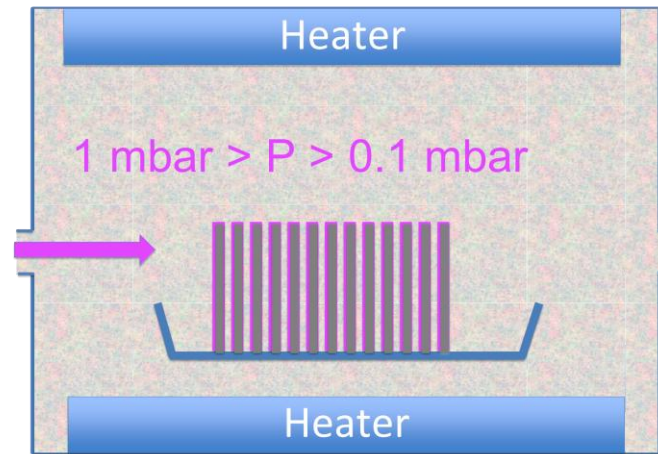
iplas CYRANNUS Microwave Plasma CVD (MPCVD) system for Diamond Growth

https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/

Simplified CVD process



- A batch of Si wafers is positioned in a fused silica holder.
- After closing of entrance port, the carrier gas enters the deposition chamber under very controlled flow and temperature conditions.



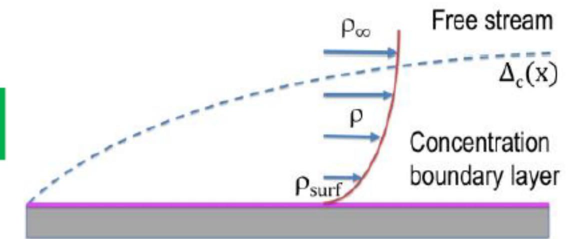
- The CVD thin film is grown on all exposed surfaces of the wafers.
- *Note: Wafers can be stacked vertically in batches due to homogeneous gas conditions, e.g., LPCVD.
- Enhanced wafer throughput.

See MOOC:
Overview of CVD techniques

Now let's have a closer look of the reaction

- Mass transfer from gas phase to substrate

- At equilibrium, the concentration at the surface (y=0) is maintained at a uniform value $\rho_{surf} < \rho_{y=\infty}$ and the gas transfer rate per unit surface can be written in three dimensions as



$$\dot{N}[m^{-2}s^{-1}] = h[m\,s^{-1}]\left(\rho_{surf} - \rho_{y=\infty}\right)[m^{-3}]$$

with h the mass transfer coefficient

- If mass flux associated with species transfer is by **diffusion, Fick's law** applies at the surface

$$\dot{N} = -D\left.\frac{\partial\rho}{\partial y}\right|_{y=0} \qquad h = \frac{-D\left.\frac{\partial\rho}{\partial y}\right|_{y=0}}{\left(\rho_{surf} - \rho_{y=\infty}\right)}$$

See MOOC: Theoretical aspects of CVD

Reference: Lecture note from Prof. Martin A. M. Gijs

Diffusion vs. surface reaction

- Diffusion flux of molecules through the boundary layer

$$\dot{N}_1 [m^{-2} s^{-1}] = h[m\, s^{-1}] \left(\rho_{surf} - \rho_{y=\infty}\right)[m^{-3}]$$

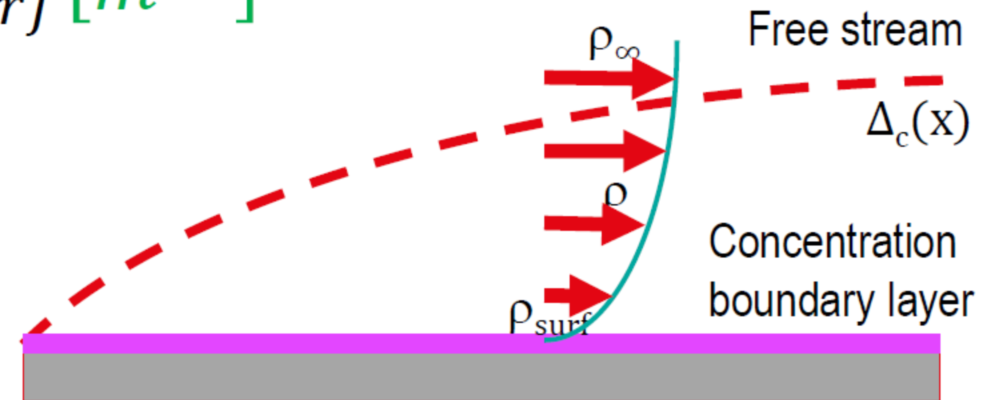
- Flux of reacted molecules consumed by the surface reaction

$$\dot{N}_2 [m^{-2} s^{-1}] = -k_{surf} [m\, s^{-1}] \rho_{surf} [m^{-3}]$$

with k_{surf} the surface reaction rate

- In equilibrium, $\dot{N} \equiv \dot{N}_1 = \dot{N}_2$, giving

$$\rho_{surf} = \rho_{y=\infty} \left(\frac{h + k_{surf}}{h}\right)^{-1}$$



Arrhenius plot of the film growth rate

- The film growth rate is then proportional to

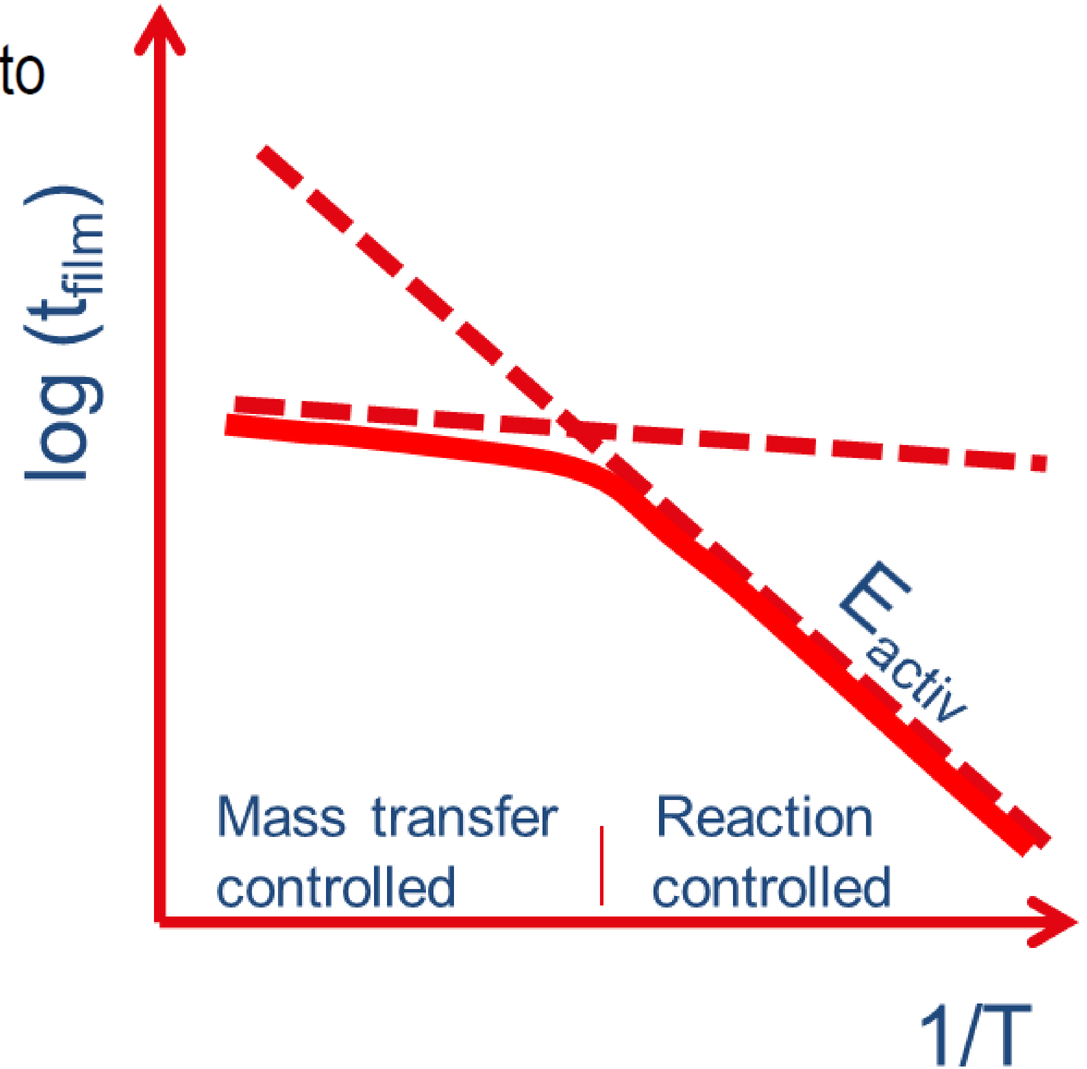
$$\dot{N} = \frac{k_{surf} h}{h + k_{surf}} \rho_{y=\infty}$$

- If $h \gg k_{surf}$, we have the surface reaction-controlled case and

$$\dot{N} = k_{surf} \, \rho_{y=\infty}$$

- If $h \ll k_{surf}$, we have the diffusion-controlled case and

$$\dot{N} = h \, \rho_{y=\infty}$$



Why temperature dependent?

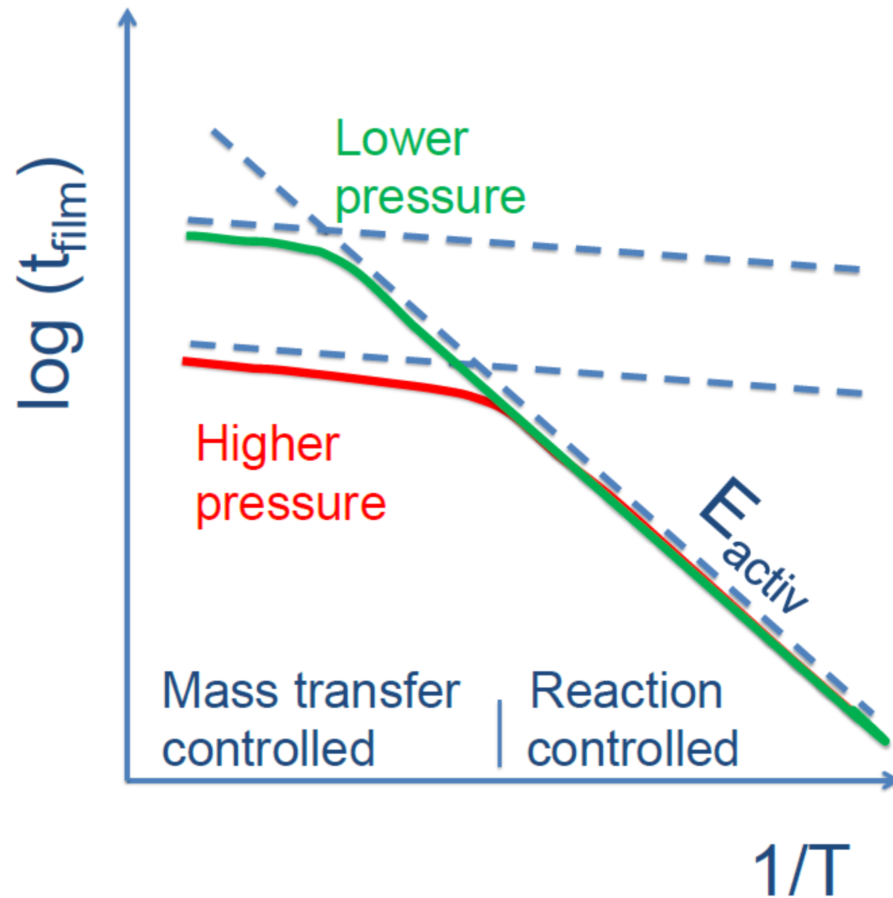
- Thickness of thin film grown by CVD

$$t_{film}(x) = C_{gas}(x) \cdot P_{growth} \cdot exp\left(-\frac{E_a}{kT}\right) \quad \sim k_{surf}$$

$C_{gas(x)}$ Concentration of the gas molecules
P_{growth} Represents the thin film growth kinetics
E_a Activation energy
T **Temperature**
k Boltzmann's constant

- Temperature decides whether film growth is in the reaction-limited or gas diffusion-limited regime
  - At high temperature, growth is in the mass transport-limited regime
    - Control of gas flow and pressure is crucial for obtaining uniform films
  - At low temperature, growth is in the reaction-limited regime
    - Control of local temperature is crucial for obtaining uniform films

Pressure effect at high temperature



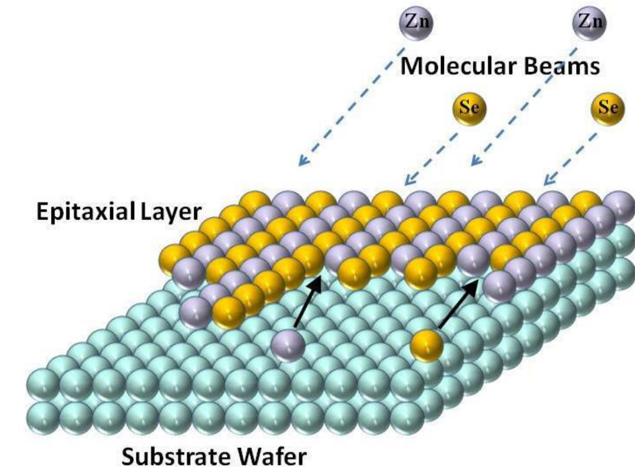
- Lower gas pressure, higher mean free path of the gas molecules, more diffusion to the substrate
  - Sub-atmospheric pressure CVD (SACVD)
  - Low-pressure CVD (LPCVD)
  - Ultrahigh vacuum CVD (UHV/CVD)
  - PECVD

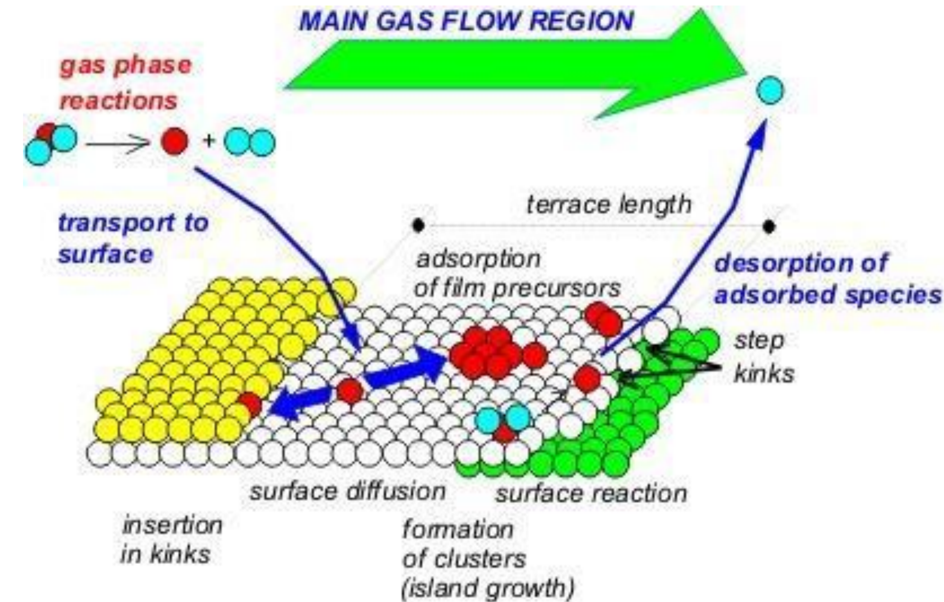
  …

See MOOC:
Overview of CVD techniques

CVD Epitaxy (basics) *Epitaxy (greek) = επι (on) + ταξψ (ordered)*

- CVD deposition process in which atoms move to lattice sites, continuing the substrate's crystal structure
  - Homoepitaxy: same material, i.e., Si on Si
  - Heteroepitaxy: different materials, i.e., AlGaAs on GaAs
- How it happens
  - Slow deposition rate (enough time to find a lattice site)
  - High temperature (enough energy to move to a lattice site)
- Selective epitaxy is possible through masking
- Can grow a doped Si layer of known thickness
- Metalorganic chemical vapor deposition (MOCVD)





Reference: Lecture note from Semiconductor Physics

Absorption/desorption

☞ Physisorption:

no chemical interaction involved (van der Waals).

E_a ~ 100 meV/atom

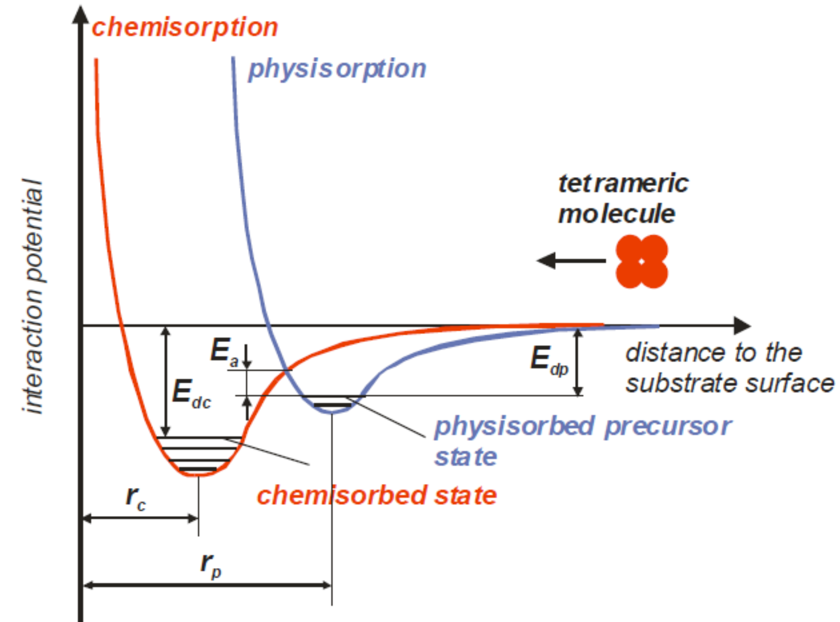
☞ Chemisorption:

strong chemical bond formed.

E_a ~ a few eV/atom

(> substrate sublimation energy)

We will revisit this in PVD

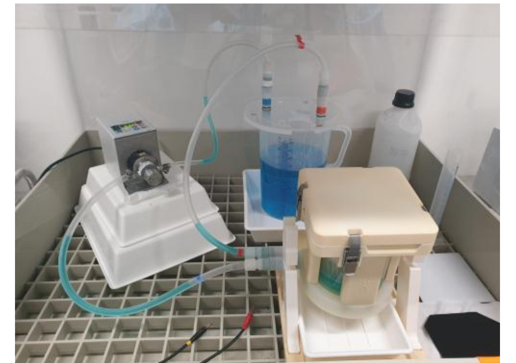


Reference: Lecture note from Semiconductor Physics

Electroplating (basics)

- Pass a current through an aqueous metal solution
  - Anode is made of the metal that you want to deposit
  - Cathode is the conductive seed material on your wafer
  - Positive metal ions travel to the negatively charged cathode on your wafer and deposit there
- Preparing your wafer
  - If you want to plate metal in some places and not in others, you will need a patterned metal seed layer (and typically a ‘sticky’ metal adhesion layer under that)
  - For very short features, just plate onto the seed layer
  - For taller features, need to plate into a mould
  - Moulds can be photoresist, silicon, SU-8, etc., depending on the needs of your device

Silicet, electroplating system for Cu
Image from CMi



Today's program

- 1st hour:
  - Feedback of the SLT_1 (10')
  - Recapitulation: MEMS (10')
  - Recapitulation: Cleanroom (10')
  - Process flow (10')
  - Q&A (5')

- 2nd hour:
  - Chemical vapor deposition (CVD) (40')
  - Q&A (5')

Take home messages

- MEMS: A balance between academic curiosity and commercial success
- Cleanroom: air, temperature, humidity, media, cloth, tools…
- Thermal oxidation
- CVD: chemical gas-phase reaction + deposition
- Diffusion vs. surface reaction
- Arrhenius plot of the film growth rate

Course plan

- Tomorrow (Thu / 2 Oct):
  - MOOC self-study, lecture room is available, MOOC: **CVD**

- Next week:
- Wed / 8 Oct
  - SLT_#2 in groups, Topic: CVD
- Thu / 9 Oct
  - MOOC self-study, lecture room is available, MOOC: **PVD**
- Wed / 15 Oct
- **Lecture**, Topic: CVD recap, PVD, and other deposition techniques

See you next time!

Speaker